

ABSTRACT OF THE DISCLOSURE

A distributed processing system includes a cache coherency mechanism that essentially encodes network routing information into sectorized presence bits. The mechanism organizes the sectorized presence bits as one or more arbitration masks that
5 system switches decode and use directly to route invalidate messages through one or more higher levels of the system. The lower level or levels of the system use local routing mechanisms, such as local directories, to direct the invalidate messages to the individual processors that are holding the data of interest.

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